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DAMASCENE PROCESS CAPABLE OF AVOIDING VIA RESIST POISONING

Abstract

A method for avoiding resist poisoning during a damascene process is disclosed. A semiconductor substrate is provided with a low-k dielectric layer ($k \leq 2.9$) thereon, a SiC layer over the low-k dielectric layer, and a blocking layer over the SiC layer. The blocking layer is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer from contacting an overlying resist. A bottom anti-reflection coating (BARC) layer is formed on the blocking layer. A resist layer is formed on the BARC layer, the resist layer having an opening to expose a portion of the BARC layer. A damascene structure is formed in the low-k dielectric layer by etching the BARC layer, the blocking layer, the SiC layer, and the low-k dielectric layer through the opening.